

1st
Edition

Parallel Test Technology

The New Paradigm for Parametric Testing



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Parallel Test Technology: The New Paradigm for Parametric Testing

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KEITHLEY

Foreword

As the dimensions of modern integrated circuits continue to shrink and the use of innovative materials grows, device fabrication and parametric testing have become more challenging with each passing year. Every device shrink, every process innovation, and every new material has made the repeatability and volume of data produced by parametric test more critical to process development and controlling modern fabs. Today's fabs must understand how to produce and characterize materials like high κ gate dielectrics and the low κ insulators used in conductive layers quickly and cost-effectively; tomorrow's IC producers may well need to learn how to manufacture and test transistors formed from carbon nanotubes or other technologies that researchers have only begun to imagine.

This book offers a high level overview of how parallel parametric testing can help today's highly automated, 24/7 fabs maximize the throughput of their existing parametric test hardware and reduce their cost of test. But parallel test has the potential to do much more than help fabs reduce the cost of ownership for their parametric test equipment. By extracting more data from every probe touchdown, parallel test offers fabs the flexibility to choose whether they want to increase their wafer test throughput dramatically or to use the time to acquire significantly more data, so they can gain greater insight into their processes than ever before.

I hope you find this book as informative and enlightening as I have during the development and review process. And best of luck with your parallel test implementation journey!

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SECTION I**What is Parallel
Parametric Test?**

Introduction

The shortest, simplest definition of parallel parametric test is that it's an emerging strategy for wafer-level parametric testing that involves concurrent execution of multiple tests on multiple scribe line test structures. It offers enormous potential for increasing test throughput with existing test hardware.

The market pressure to minimize test times is the most powerful motivator driving fabs to explore parallel testing. It offers a relatively inexpensive way to increase throughput, thereby lowering the Cost of Ownership significantly. Just as important, parallel testing can address the growing need to perform more tests on the same structures in less time as device scaling increases the randomness of failures.

As of this writing (2006), the structures being tested in parallel are typically located within a single Test Element Group (TEG). Even among leading-edge IC manufacturers, very few have progressed to the point of testing structures in different TEGs simultaneously. Implementing this strategy involves using the tester's controller to inter-leave execution of the multiple tests in a way that maximizes the use of processing time and test instrumentation capacity that would otherwise be standing idle. When the design of the test structures allows, this "multi-threaded" approach to test sequencing reduces the execution time for multiple tests on multiple structures to little more than the time needed to execute the longest test in the sequence.

Parallel test vs. traditional sequential mode approach

To illustrate the throughput advantage that parallel testing offers, it may be helpful to contrast it with the traditional approach to parametric test, in which each test in the sequence must be completed before the next one can begin. The total test time for an individual TEG is approximately the sum of the test times for the individual test devices, plus any delays due to switching latencies, which can be significant.

Today's parametric test systems can be equipped with up to eight Source-Measure Units (SMUs), although most systems have fewer installed. However, for the sake of argument, if a tester configured with eight SMUs was operated in sequential mode for simple tests such as measuring a resistor (which requires one SMU for the two nodes), then seven SMUs would be sitting idle. Parallel test increases utilization of both the tester and prober and boosts throughput by measuring multiple devices simultaneously. (**Figure 1-1** illustrates the difference between the amounts of time required to perform a set of tests sequentially vs. the same tests performed realistically in parallel.)

Devices tested in parallel may be of all the same type (homogenous) or of different types (heterogeneous). For example, two transistors, one resistor, and one diode could potentially be measured independently and asynchronously by performing different connect-force-measure sequences on all four devices simultaneously. **Figures 1-2** and **1-3** illustrate the difference between how tests within a single TEG are tested in sequen-

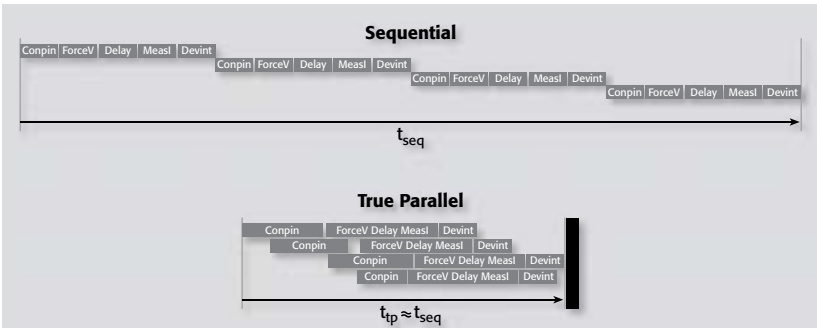


Figure 1-1. Sequential mode vs. parallel test timing.

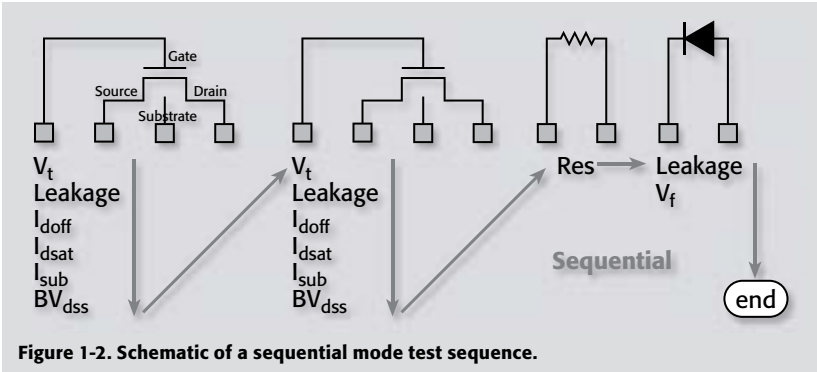


Figure 1-2. Schematic of a sequential mode test sequence.

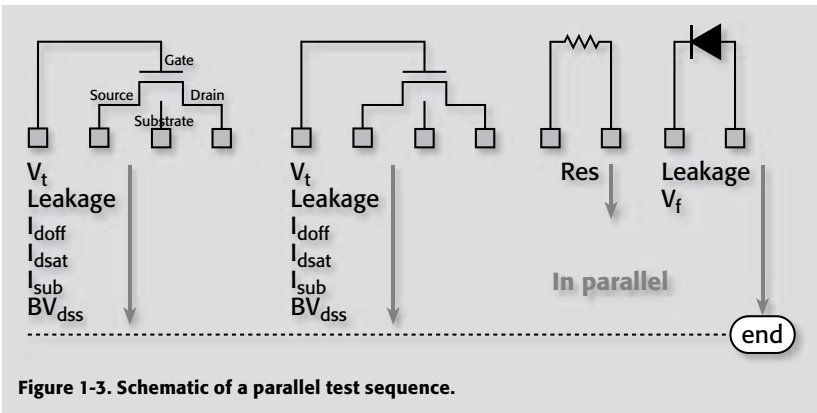


Figure 1-3. Schematic of a parallel test sequence.

tial mode and in parallel mode. Note how the parallel mode test sequence maximizes the use of the instrument resources available.

Wafer-level parallel parametric test vs. parallel functional test

Although the concept of parallel test has been discussed extensively in the semiconductor industry over the last few years, many of those discussions focus on parallel functional testing of packaged components, rather than on wafer-level parallel parametric test. For example, Keithley's Model 4500-MTS Multi-Channel I-V Test System and Series 2600 System SourceMeter® Multi-Channel I-V Test Solutions can be applied to parallel functional test applications. Keithley's S680 Automatic Parametric Test Systems falls into the true parallel parametric test category.

Although both types of parallel testing use a similar testing strategy (i.e., the use of multiple SMUs operating asynchronously to reduce total test time), there are obvious differences. The most significant one, other than the size and cost of the test hardware itself, is that functional tests of packaged devices are largely immune to the parasitic capacitances between devices under test that can interfere with parametric test accuracy, whether those tests are performed sequentially or in parallel. Parallel functional testing with the Model 4500-MTS or the Series 2600 instruments also support the use of channel groups for testing multiple devices and eliminating further tests on failed devices, which parallel parametric test does not. Series 2600 instruments can also be grouped through the use of multiple GPIB addresses. These groups of SMUs, each with a master unit and one or more slaves, can execute tests in the same asynchronous, concurrent fashion as the Model 4500-MTS's channel groups.

The parallel test continuum

When discussing parallel test strategies, it's important to remember not all fabs (or even all test cells within the same fab) should necessarily implement it in the same way. Rather than a single approach to parallel test implementation, it's more productive to think of parallel test implementation as a continuum. The point on this continuum that's most appropriate for a particular fab or test cell will depend on a number of factors, including the manufacturing technology, the maturity of its production process and TEGs, and its anticipated manufacturing lifespan (i.e., how long the fab will continue to produce it). The following paragraphs describe the end points and midpoint of this implementation continuum:

- **Picking the “low hanging fruit”:** For many fabs or test cells working with mature processes, this approach to parallel test will be the most attractive because it involves changing only the test sequencing on existing TEGs. Typically, this would require analysis of both the TEG and the test sequence to identify opportunities for reordering or regrouping existing tests on heterogeneous structures in a way that minimizes the time needed for switching

between test pads. A majority of the discussion in this book will focus on this approach because it represents the fastest, surest way for fabs to achieve significant throughput improvements with a relatively limited investment in analysis effort, new software, and test sequence modifications.

- **Doing the heavy lifting:** This point in the continuum demands much more extensive analysis of both the test sequence and the TEG itself because it requires significant changes to both. A number of new reticles typically must be designed, created, and validated to allow parallel testing of more structures within the TEG. This point in the parallel test continuum may also require changes to the probe card design, as well as the installation of additional source-measure instrumentation. While it's important for prospective users to understand the expense and time required at this point in the continuum, for many fabs, the throughput gains parallel test makes possible may justify the effort.
- **Plowing the "green field":** During technology development for new products, it's relatively inexpensive to design the new TEGs in a way that maximizes the number of structures that can be tested in parallel. Given that there are no existing reticles or test sequences that must be replaced, there's no existing testing process to disrupt. While this point in the continuum offers the highest potential for payback in terms of throughput, it's wiser not to try implementing parallel test for the first time on a new product, when there are many other priorities to consider while trying to ramp up production. Instead, the knowledge gained from first implementing parallel test on mature processes using the "low hanging fruit" approach can be applied to the process of implementing it on new products later. Parametric test vendors can also provide enormous assistance by reviewing test structures and algorithms, which may make it possible to ramp parallel test technology significantly faster.

Weighing the advantages of parallel test

Parallel parametric test offers a variety of advantages over traditional sequential parametric testing:

- **Cost of ownership advantages.** The most obvious advantage of parallel test is its impact on the cost of ownership (COO) of the parametric test system on which it is implemented. The largest "lever" on the cost of ownership for a process or metrology tool is system throughput; therefore, by increasing throughput, parallel test decreases the system's cost of ownership. Users have documented throughput increases due to parallel test ranging from

1.05× to 3.9×. The degree of throughput improvement that a particular fab or test cell can achieve will depend on a variety of factors:

- *The existing test structure and pad layout.* When designing scribe line test structures, saving space has long been an important objective for many TEG designers. In order to minimize the amount of costly wafer real estate devoted to TEGs, designers have typically designed structures with shared gate pads, which can make it impossible to test certain structures in parallel.
- *The specific combination of test structures within the TEG.* Consider, for example, a structure made up of an array of transistors, all of which share a single gate pad. It would be impossible to characterize the devices fully within such a structure in parallel. Conversely, a resistor network would likely allow testing of all the resistors in parallel because such a structure would have a pad at every node in the network, allowing the tester to source current across the whole network, then measure the voltage drop at each node. Most TEGs, however, fall somewhere in between these two extremes. A more likely scenario is a TEG that includes at least one capacitor, one resistor, one diode, and one transistor. Although some of these test structures may, in fact, share pads, some level of parallel testing is still achievable. For example, it might be possible to measure the forward voltage drop of a diode and the resistance of a resistor in parallel, even if they are connected in series, as long as there is a pad at the node where the two structures connect. Similarly, it's likely that one can measure the resistance of a polysilicon line, the leakage of a capacitor, and the reverse leakage of a diode in parallel. Typically, however, C-V measurements are performed sequentially, largely because few testers are equipped with more than one C-V meter. There are also lingering concerns about the potential for C-V measurements to create parasitic coupling with nearby structures or probe tips if performed in parallel with other measurements.
- **Test cell capacity advantages.** Parallel test can be a good option for fabs with limited make-up test capacity and that lack the resources and/or the floor space to add another test cell. By allowing fabs to use their existing testing hardware more efficiently, parallel test can often eliminate the need for additional test cells or reduce the number of test cells needed when equipping a new fab.
- **Impact on overall cost of test.** Parallel test users have reported a variety of other benefits that helped reduce their overall cost of parametric test:

Parallel test vs. adaptive test

When weighing alternatives for improving parametric test throughput, fab managers often consider an adaptive testing strategy rather than parallel testing. While both represent valid approaches for reducing cost of ownership, they are very different in nature. A brief overview of adaptive testing may be helpful in understanding these differences.

Results-based adaptive testing allows programming the tester to increase or decrease the number of sites tested and the number of tests performed on a wafer based on the results of previous measurements. If the results from previous sites are acceptable, the number of sites and/or tests can be reduced, thereby increasing throughput when testing good wafers. When previous test results don't meet the pre-set criteria, adaptive test supports several different scenarios. If the test is used for process control, the tester can make extensive additional tests at the bad sites automatically (more tests, same TEG), so that a more complete set of parameters is available for analysis by the process engineer if the lot is placed on hold. When used for lot dispositioning, the tester can perform the same tests at all die on the wafer automatically (same tests, more die), to determine known good die for final test. In either case, adaptive test can largely reduce or eliminate the time, expense, and errors involved in re-probing.

Most parallel parametric test experts would advise test managers against attempting to ramp up both parallel testing and adaptive testing at the same time because these techniques are based on differing strategies, even though both are designed to increase test throughput. Adaptive test requires setting thresholds that define what constitutes an acceptable or unacceptable wafer. Unacceptable wafers can trigger 100% testing of the remainder of the lot in order to gather additional data, which the process engineer can use in tracking down the source of the problem. In contrast, parallel testing, by clustering tests and structures for improved efficiency, already provides a larger data sample in less time, without relying on adaptive testing's reduced sampling strategy. Implementing either strategy can be a relatively complex and time-consuming process that may require a good amount of a test manager's attention for several months. Generally, it's preferable to implement parallel test first, to ensure that the test content is stable.

Serial sequential testing of multiple structures within a TEG results in the highest quality parametric measurements. Parasitic coupling can degrade some parallel measurements to some degree. Given that the process is not optimized to control parasitic coupling behaviors, the variability of the parasitic coupling results in a broader statistical distribution of parametric measurement results. This broader distribution could trigger adaptive testing to increase sampling. The adaptive test parameters may need to be adjusted to compensate for the broader statistical distributions.

- *Reduction in number of test cells required.* Consider a hypothetical fab with three test cells that's facing a significant increase in demand for testing capacity due to the addition of a new product or ramped up production of an existing one. By boosting the throughput of each test cell by 30%, parallel test can make it unnecessary to add another cell.
- *Additional make-up capacity at relatively little cost.* Even fabs with a relatively steady demand for test capacity need make-up capacity to

accommodate disruptions like periodic tool maintenance, yield crashes, etc. Parallel testing offers the flexibility to handle these disruptions without the expense of additional test cells.

- *Reduction in the number of operators needed due to reduction in number of test cells needed and associated training required.* Fewer test cells require fewer operators—it's as simple as that. Fabs also save because fewer operators typically require fewer man-hours of training to maintain their skills.
- *Flexibility to test more extensively as desired.* The additional test capacity parallel test provides affords some fabs the time they need to add more tests to the test sequence, which may not have been possible previously. The ability to gather more information in less time helps fabs gain a better understanding of their processes.
- *Reduced consumables costs.* Fewer testers require fewer consumable items, such as probe cards.

To evaluate the effect of parallel testing on a specific operation's overall Cost of Test, Keithley recommends Wright, Williams, and Kelly's TWO COOL® for Wafer Sort & Final Test software for semiconductor test floor operations.

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